SSI

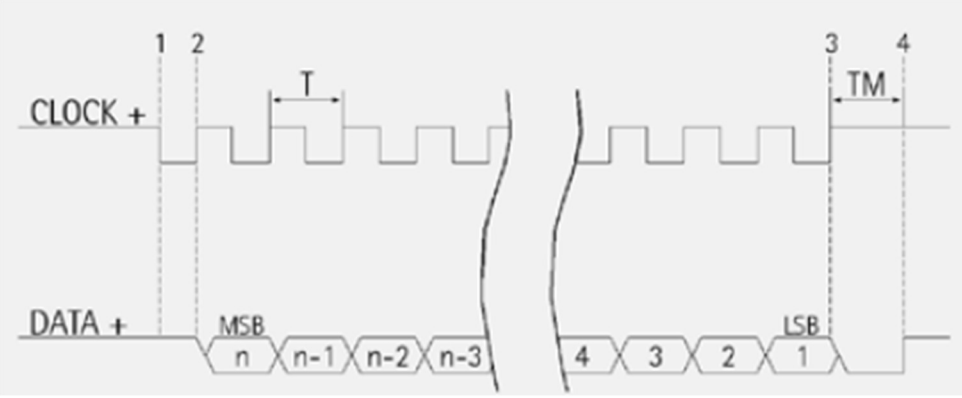
SSI (the acronym for Synchronous Serial Interface) is a synchronous point-to-point serial interface engineered for unidirectional data transmission between one Master and one Slave. Developed in 1984, it is based on the RS-422 serial standard. The data transmission is achieved by synchronizing both the Master and the Slave devices to a common clock signal generated by the controller; in this way the output information is clocked out at each controller's request. Furthermore, only two pairs of twisted wires are used for data and clock signals, thus a six-wire cable is required.

The main advantages in comparison with parallel or asynchronous data transmissions are:

- less conductors are required for transmission.
- less electronic components.
- possibility of insulting the circuits galvanically by means of optocouplers.
- high data transmission frequency.
- hardware interface independent from the resolution of the absolute encoder.

Furthermore, the differential transmission increases the noise immunity and decreases the noise emissions. It allows multiplexing from several encoders; thus, process controls are more reliable with simplified line design and easier data management.

Data transmission is carried out as follows. At the first falling edge of the clock signal (1, the logic level changes from high to low) the absolute position value is stored while at the following rising edge (2) the transmission of data information begins starting from the Most Significant Bit (MSB).



Gapp Automation Ltd
6 Kempston Court
Kempston Hardwick
Bedford
MK43 9PQ

Tel: +44 (0)1234 924324
Fax: +44 (0)1234 924325
Web: www.gapp.co.uk
Email: info@gapp.co.uk
Email: sales@gapp.co.uk

At each change of the clock signal and at each subsequent rising edge (2) one bit is clocked out at a time, up to Least Significant Bit (LSB), so completing the data word transmission.

The cycle ends at the last rising edge of the clock signal (3). This means that up to n + 1 rising edges of the clock signals are required for each data word transmission (where n is the bit resolution); for instance, a 13-bit encoder needs 14 clock edges.

If the number of clocks is greater than the number of bits of the data word, then the system will send a zero (low logic level signal) at each additional clock, zeros will either lead (LSB ALIGNED protocol) or follow (MSB ALIGNED protocol) or lead and/or follow the data word (TREE FORMAT protocol). After the period Tm monoflop time, having a typical duration of 12 µsec, calculated from the end of the clock signal transmission, the encoder is then ready for the next transmission and therefore the data signal is switched high.

SSI interface has a frequency of data transmission ranging between 100 kHz and 2 MHz. The clock frequency (baud rate) depends on the length of the cable and must comply with the technical information reported in the following table:

Max. cable length m [ft] @	400 [1310]	200 [655]	100 [330]	60 [200]	30 [100]	15 [50]
Clock frequency [kHz]	100	200	300	500	900	1800

At ambient Temperature (23°C)

The clock signal has a typical logic level of 5V, the same as the output signal which has customarily a logic level of 5V in compliance with RS-422 standard. If the single-turn resolution is lower than 13 bits, then the protocol will provide 13 clock signals (+1 edge, as stated); if the single-turn resolution is higher than 13 bits, then the protocol will provide 25 clock signals instead. Multi-turn encoders provide either 25 or 32 clock signals according to the length of the data word (bit resolution). The output code can be either Binary or Gray.

For more information on Binary and Gray code, see the dedicated white paper.

The next paper will look a little more closely at the Protocol used in SSI.

Gapp Automation Ltd
6 Kempston Court
Kempston Hardwick
Bedford
MK43 9PQ

Tel: +44 (0)1234 924324
Fax: +44 (0)1234 924325
Web: www.gapp.co.uk
Email: info@gapp.co.uk
Email: sales@gapp.co.uk